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10EC047

M.Tech. Degree Examination, June/July 2011
Low Power VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the need for low power VLSI design. **(06 Marks)**

b. What are the various sources of power dissipation in digital ICs? **(04 Marks)**

c. With usual notations show that the short circuit power dissipation in a CMOS inverter is given by, $P_{SC} = \frac{\beta}{12}(V_{DD} - V_T)^3 \frac{\lambda}{T}$ **(10 Marks)**

2 a. With the neat diagram, explain the dual bit type signal model for DSP system. Explain how data path module is characterized for a module with one input and one output such as FIFO queue with relevant capacitance and power expressions. **(10 Marks)**

b. Explain the concept of statistical estimation mean in Monte Carlo simulation technique. Derive the expressions for number of samples N required to decide the stopping criteria of simulation. **(10 Marks)**

3 a. List the advantages and limitations of SPICE power analysis method. **(06 Marks)**

b. Explain how event characterization technique can be used to compute the static state power dissipation of logic gate. **(08 Marks)**

c. Explain the gate induced drain leakage (GIDL) current in MOSFET. **(06 Marks)**

4 a. Derive the expression for conditional probability and frequency. **(08 Marks)**

b. Compute the transition density and static probability of the boolean function $y = ab + c$. Given $P(a) = 0.2$, $P(b) = 0.3$, $P(c) = 0.4$, $D(a) = 1$, $D(b) = 2$, $D(c) = 3$. **(12 Marks)**

5 a. Explain the gate level power analysis using transition density. **(06 Marks)**

b. Explain the power dissipation of the combinational circuit using entropy analysis. **(08 Marks)**

c. A 32 bit off-chip bus operating at 5V and 66 MHz clock rate is driving a capacitance of 25 PF/bit. Each bit is estimated to have toggling probability of 0.25 at each clock cycle. What is the power dissipation operating the bus. **(06 Marks)**

6 a. Explain the single driver v/s distributed buffers. **(10 Marks)**

b. With the help of relevant diagram and equations explain the concept of bus invert encoding. **(10 Marks)**

7 a. Explain the chip and package co design of clock network with relevant block diagram. **(10 Marks)**

b. What are zero skew and tolerable skew? Briefly explain buffer inversion and sizing method used to minimize wire width and meet the tolerable skew constraints. **(10 Marks)**

8 a. Explain pre-computation architecture based on Shannon's decomposition. **(08 Marks)**

b. Define signal gating. Explain the various logic implementations of signal gating. **(08 Marks)**

c. Write a note on body effect of long-channel MOSFET. **(04 Marks)**